

REMARKS

The above amendments and following remarks are submitted in response to the Official Action of the Examiner mailed November 14, 2004 (i.e., Paper No. 11). Having addressed all objections and grounds of rejection, claims 1-20, being all the pending claims, are now deemed in condition for allowance. Entry of this amendment and reconsideration to that end is respectfully requested.

The Examiner has rejected claim 2 as containing a typographical error. Claim 2 has been amended above in response to this objection.

The Examiner has rejected claims 1-3, 6, 10-12, and 16-17 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,314,491, issued to Freerksen et al (hereinafter referred to as "Freerksen"). This ground of rejection is respectfully traversed as to the claims herein amended.

Claims 1, 6, 11, and 16 have been herein amended to limit them to an environment having dual level one cache memories (i.e., instruction cache memory and operand cache memory). Furthermore, the level one operand cache memory is a "store-through" cache memory having no need of a "flush buffer". The

level one instruction cache memory is read-only, so it also does not need a "flush buffer". As a result, only the claimed "store-in" cache memory is coupled to the "flush buffer", because it is the only element experiencing the need for flushing. This is readily distinguishable from Freerksen, which is characterized by the Examiner stating:

intermediate cache buffer 30 is directly coupled to L1 caches 28a, 28b; to L2 cache 26 and main storage 14; Fig. 2; data is cast back into cache buffer 30 which is an intermediate storage area; col. 6, lines 41 - col. 7, line 4.

As a result, L1 caches 28a and 28b, must either be "store-in" cache memories or intermediate cache buffer 30 is not a flush buffer as defined and claimed by Applicants.

In his rejection of claim 2, the Examiner states that the L1 cache memories of Freerksen are store-in cache memories citing line 52 of Fig. 4. Column 4, lines 19-20 states:

FIG. 4 is a block diagram of the contents of the L1 caches illustrated in FIG. 2;

The rejection of claims 1 and 2, as amended, is respectfully traversed.

The rejection of claim 10, as amended, is respectfully traversed as a matter of law. It now depends from claim 9, and therefore contains all of the limitations of claim 9.

Claim 11 has been further amended which directly impacts the flow of data and control signals. As a result, claim 11 cannot

be anticipated by Freerksen. The rejection of claim 11, as amended, is respectfully traversed.

The rejection of claim 16, as amended, is respectfully traversed. Freerksen does not have the claimed "handling means".

Claims 4-5, 7-9, 14-15, and 18-20 have been rejected under 35 U.S.C. 103(a) as not patentable over an alleged combination including U.S. Patent No. 6,460,114, issued to Kurosawa (hereinafter referred to as "Kurosawa"). The Examiner has recited Kurosawa to show the "double buffering" limitation applied to the claimed "flush buffer". He states, for example:

[Kurosawa's] data is registered in the write-back buffer 403 at the second stage when write-back buffer 402 becomes free.

A review of Fig. 2 shows that all write back data must be routed through buffer 403, thus not benefitting from the benefits of double buffering described by Applicants at page 16, lines 14-19. Therefore, claims 4 and 7 have been amended to more explicitly require this structure. The remaining claims are deemed to be already so limited without further amendment.

Having thus responded to each objection and ground of rejection, Applicants respectfully request entry of this amendment and allowance of claims 1-20, being the only pending claims.

Respectfully submitted,

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By their attorney,

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